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REMARKS

The following remarks are made in response to the Office Action mailed June 13, 2006. Claims 1-73 were rejected. With this Amendment and Response, claims 1, 35, 36, 40, 44, 46, 47, 49, 61, 63, and 64 have been amended. Claims 43, 48, and 69-73 have been cancelled without prejudice. Claims 1-42, 44-47, and 49-68 remain pending in the application and are presented for reconsideration and allowance.

Claim Objection

The Examiner objected to the numbering of claims because the number of claims is not in accordance with 37 C.F.R. 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution.

The claims have been presented as renumbered by the Examiner.

Claim Rejections under 35 U.S.C. § 102

Claims 1, 2, 4-6, 9-15, 30-32, 35, 37, 38, 50, 51, 54-56, 59 and 60 were rejected under 35 U.S.C. § 102(b) as being anticipated by Skene et al. U.S. Publication No. 2002/0175965, (the Skene et al. publication).

Claim 73 was rejected under 35 U.S.C. § 102(b) as being anticipated by Aono et al. U.S. Publication No. 2002/0145645.

The Skene et al. publication is directed to a system and method for detecting an error in data received from a memory of a replaceable printer component. The printer includes a plurality of electrically conductive lines and the memory includes a plurality of bits. At least one of the electrically conductive lines is associated with each bit. A first data item and a first parity bit are read from the memory and an electrical test of at least one of the electrically conductive lines is performed. An error in the first data item is identified based on the first parity bit read from the memory and the electrical test.

Applicant respectfully submits that the Skene et al. publication fails to teach or suggest identification cells, wherein each of the identification cells comprises a memory circuit and a memory element, as recited in amended independent claim 1. In contrast, in the Skene et al. publication, the circuit for defining the state of a fusible bit and the circuit for defining the state of a masked bit, each include non-storage circuit elements, and a fusible bit or a masked bit.

The Skene et al. publication also fails to teach or suggest a memory circuit adapted to receive and respond to signals to selectively store a value in the memory circuit, wherein the value determines whether the identification cell is responsive to signals received on the identification line to perform at least one of the following: read the memory element; and program the memory element, as recited in amended independent claim 1. In addition, the Skene et al. publication fails to teach or suggest storing the enabling value that selectively enables the identification cell to be programmed via the program signal and read via the read signal, as recited in independent claims 50 and 56. In contrast, in the Skene et al. publication, the circuit for defining the state of a fusible bit and the circuit for defining the state of a masked bit, each include a transistor coupled to an enable input and an address input that are set high to sense the signal at the output of the circuit. The transistor coupled to the enable input and the address input acts as an AND gate to turn on another transistor coupled to the fusible bit or the masked bit.

The Skene et al. publication also fails to teach or suggest a group of data lines, wherein the group of data lines is configured to receive data representing an image and signals that selectively enable identification cells, as recited in amended independent claim 35. In contrast, in the Skene et al. publication, the circuit for defining the state of a fusible bit and the circuit for defining the state of a masked bit are each coupled to enable inputs and an address input.

The Skene et al. publication also fails to teach or suggest identification cells, wherein each of the identification cells is coupled to at least two data lines in the group of data lines, as recited in amended independent claim 35. In addition, the Skene et al. publication fails to teach or suggest identification cells adapted to conduct and respond to signals transmitted on the at least two data lines to be selectively enabled, wherein each enabled identification cell is adapted to be programmed via the program signal and read via the read signal, as recited in amended independent claim 35. In contrast, the circuit for defining the state of a fusible bit and the circuit for defining the state of a masked bit, each include transistors coupled to enable inputs and an address input, wherein an enable input and an address input are set high to sense the signal at the output of the circuit.

In view of the above, Applicant submits that all features of amended independent claim 1, all features of amended independent claim 35, all features of independent claim 50,

and all features of independent claim 56, are not taught or suggested by the Skene et al. publication.

As dependent claims 2, 4-6, 9-15, 30-32 further define patentably distinct amended independent claim 1, and dependent claims 37 and 38 further define patentably distinct amended independent claim 35, and dependent claims 51, 54, and 55 further define patentably distinct independent claim 50, and dependent claims 59 and 60 further define patentably distinct independent claim 56, these dependent claims are also believed to be allowable.

Claim 73 has been cancelled without prejudice.

Therefore, Applicant respectfully requests reconsideration and withdrawal of the 35 U.S.C. § 102 rejections and allowance of these claims.

Claim Rejections under 35 U.S.C. § 103

Claim 3 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Skene et al. U.S. Publication No. 2002/0175965.

Claim 7 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Skene et al. U.S. Publication No. 2002/0175965 in view of Kao et al. U.S. Publication No. 2002/0057305.

Claims 8, 16-19, 44-46, 52, 53, 57, 58 and 61-66 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Skene et al. U.S. Publication No. 2002/0175965 in view of Axtell et al. U.S. Publication No. 2002/0060722, (the Axtell et al. publication).

Claims 20-23, 25 and 28 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Skene et al. U.S. Publication No. 2002/0175965 in view of Inose U.S. Patent No. 6,385,407.

Claim 24 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Skene et al. U.S. Publication No. 2002/0175965 in view of Pawelka et al. U.S. Patent No. 5,886,726.

Claim 26 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Skene et al. U.S. Publication No. 2002/0175965 in view of Heim et al. U.S. Patent No. 6,431,673.

Claim 27 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Skene et al. U.S. Publication No. 2002/0175965 in view of Miller U.S. Publication No. 2003/0146967.

Claims 29, 40, 42 and 43 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Skene et al. U.S. Publication No. 2002/0175965 in view of Bolash et al. U.S. Patent No. 6,081,280, (the Bolash et al. patent).

Claims 33, 34, 36 and 39 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Skene et al. U.S. Publication No. 2002,0175965 in view of the Hayasaki reference EP 1128324.

Claim 41 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Skene et al. U.S. Publication No. 2002/0175965 and Bolash et al. U.S. Patent No. 6,081,280, and further in view of Axtell et al. U.S. Publication No. 2002/0060722.

Claims 37 and 38 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Skene et al. U.S. Publication No. 2002/0175965 and Bolash et al. U.S. Patent No. 6,081,280 and further in view of the Hayasaki reference EP 1128324.

Claims 69-72 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Skene et al. U.S. Publication No. 2002/0175965 in view of Aono et al. U.S. Publication No. 2002/0145645.

As to independent claim 44, the Examiner admits that the Skene et al. publication does not teach means for storing the enabling value that enables the identification cell to be programmed via the program signal and read via the read signal.

Applicant respectfully submits that the Skene et al. publication also fails to teach or suggest data lines for receiving data representing an image and receiving signals that selectively enable identification cells, as recited in amended independent claim 44. In contrast, in the Skene et al. publication, the circuit for defining the state of a fusible bit and the circuit for defining the state of a masked bit are each coupled to enable inputs and an address input.

In addition, the Skene et al. publication fails to teach or suggest means for responding to the signals to provide an enabling value, as recited in amended independent claim 44, where the signals are the signals on the data lines. In contrast, the circuit for defining the state of a fusible bit and the circuit for defining the state of a masked bit, each include transistors coupled to enable inputs and an address input, wherein an enable input and an address input are set high to sense the signal at the output of the circuit.

The Examiner further relies on the Axtell et al. publication as a basis for the § 103 obviousness rejection. The Axtell et al. publication is directed to a dynamic memory based integrated circuit ink jet firing cell. The firing cell includes an ink jet heater resistor, a dynamic memory circuit for storing heater resistor energizing data only for the heater resistor, and a drive transistor. The drive transistor enables a transfer of energy to the heater resistor

as a function of the state of the energizing data. Also disclosed is an integrated circuit firing array that includes a plurality of dynamic memory based firing cells divided into a plurality of fire groups.

Applicant respectfully submits that the Axtell et al. publication fails to teach or suggest data lines for receiving data representing an image and receiving signals that selectively enable identification cells, as recited in amended independent claim 44. In contrast, in the Axtell et al. publication, the data lines receive data signals and do not receive signals that selectively enable identification cells.

The Axtell et al. publication also fails to teach or suggest means for responding to the signals to provide an enabling value, as recited in amended independent claim 44, where the signals are the signals on the data lines that selectively enable identification cells. In contrast, in the Axtell et al. publication, data transistors in firing cells receive data via the data lines.

In addition, the Axtell et al. publication, fails to teach or suggest means for storing the enabling value that selectively enables the identification cells to be programmed via a program signal and read via a read signal, as recited in amended independent claim 44. In contrast, in the Axtell et al. publication, an ink firing cell includes a dynamic memory element for storing heater resistor data only for the heater resistor.

As to independent claim 61, the Examiner admits that the Skene et al. publication does not teach a second switch coupled to the first switch, the second switch discharging the first switch to prevent the memory element from responding to the signals received on the identification line. Applicant submits that the Skene et al. publication fails to teach or suggest a second switch coupled to the first switch, the second switch discharging the stored charge state of the first switch to prevent the memory element from responding to the signals received on the identification line, as recited in amended independent claim 61.

Also, the Skene et al. publication fails to teach or suggest a first switch coupled to the memory element, wherein the first switch in a stored charged state allows the memory element to respond to signals received on the identification line, as recited in amended independent claim 61. In contrast, in the Skene et al. publication, the circuit for defining the state of a fusible bit and the circuit for defining the state of a masked bit, each include a transistor coupled to an enable input and an address input that are set high to sense the signal at the output of the circuit. The transistor coupled to the enable input and the address input

acts as an AND gate to turn on another transistor coupled to the fusible bit or the masked bit. The other transistor does not have a stored charge state.

The Examiner further relies on the Axtell et al. publication as a basis for the § 103 obviousness rejection. Applicant respectfully submits that the Axtell et al. publication fails to teach or suggest a plurality of cells, each comprising a memory element coupled to an identification line, as recited in amended independent claim 61. In contrast, in the Axtell et al. publication, firing cells include a heater resistor coupled to a fire line and the firing cells receive energizing energy via the fire line.

The Axtell et al. publication also fails to teach or suggest a first switch coupled to the memory element, wherein the first switch in a stored charged state allows the memory element to respond to signals received on the identification line, as recited in amended independent claim 61. In contrast, in the Axtell et al. publication, a drive transistor is coupled to a heater resistor (not a memory element). Firing pulse energy is transferred to the heater resistor if the drive transistor is on at the time the firing pulse is present.

Also, the Axtell et al. publication fails to teach or suggest a second switch coupled to the first switch, the second switch discharging the stored charge state of the first switch to prevent the memory element from responding to the signals received on the identification line, as recited in amended independent claim 61. In contrast, in the Axtell et al. publication, transistors coupled to the drive transistor discharge the gate capacitance of the drive transistor to turn off the drive transistor, which is coupled to a heater resistor (not a memory element). If the drive transistor is off, firing pulse energy from the fire line is not transferred to the heater resistor.

As to independent claim 40, the Examiner admits that the Skene et al. publication does not teach an identification line configured to conduct a signal to detect low impedance between the identification line and each of the input pads.

Applicant submits that the Skene et al. publication also fails to teach or suggest an identification line that includes finger portions situated between adjacent input pads, as recited in amended independent claim 40. In contrast, in the Skene et al. publication, a semiconductor die includes a plurality of pads. An output line is coupled to the semiconductor die via one of the pads.

The Examiner further relies on the Bolash et al. patent as a basis for the § 103 obviousness rejection. The Bolash et al. patent is directed to a method and apparatus for

inhibiting induced ink build up on flexible, integrated circuit connecting leads, for thermal ink jet printer heads.

Applicant respectfully submits that the Bolash et al. patent fails to teach or suggest an identification line that includes finger portions situated between adjacent input pads and configured to conduct a signal to detect low impedances between the identification line and the input pads, as recited in amended independent claim 40, where the identification line is adapted to conduct a program signal to program identification information and a read signal to read identification information. In contrast, in the Bolash et al. patent, a detection circuit is shown to detect data line to ground short circuits and pre-heater to ground short circuits.

In view of the above, Applicant submits that all features of amended independent claim 44 and all features of amended independent claim 61 are not taught or suggested by the Skene et al. publication and the Axtell et al. publication, alone or in combination. Also, Applicant submits that all features of amended independent claim 40 are not taught or suggested by the Skene et al. publication and the Bolash et al. patent, alone or in combination.

As dependent claims 2-34 further define patentably distinct amended independent claim 1, dependent claims 36-39 further define patentably distinct amended independent claim 35, dependent claims 41 and 42 further define patentably distinct amended independent claim 40, dependent claims 45-47 and 49 further define patentably distinct amended independent claim 44, dependent claims 51-55 further define patentably distinct independent claim 50, dependent claims 57-60 further define patentably distinct independent claim 56, and dependent claims 62-68 further define patentably distinct amended independent claim 61, these dependent claims are believed to be allowable.

Claims 69-72 have been cancelled without prejudice.

Therefore, Applicant respectfully requests reconsideration and withdrawal of the 35 U.S.C. § 103 rejections and allowance of these claims.

CONCLUSION

In view of the above, Applicant respectfully submits that pending claims 1-42, 44-47, and 49-68 are in form for allowance and are not taught or suggested by the cited references. Therefore, reconsideration and withdrawal of the rejections and allowance of claims 1-42, 44-47, and 49-68 is respectfully requested.

Amendment and Response
Applicant: Trudy L. Benjamin et al.
Serial No.: 10/827,135
Filed: April 19, 2004
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Title: FLUID EJECTION DEVICE WITH IDENTIFICATION CELLS

No fees are required under 37 C.F.R. 1.16(h)(i). However, if such fees are required, the Patent Office is hereby authorized to charge Deposit Account No. 08-2025.

The Examiner is invited to contact the Applicants' representative at the below-listed telephone numbers to facilitate prosecution of this application.

Any inquiry regarding this Amendment and Response should be directed to either Patrick G. Billig at Telephone No. (612) 573-2003, Facsimile No. (612) 573-2005 or Donald J. Coulman at Telephone No. (541) 715-1694, Facsimile No. (541) 715-8581. In addition, all correspondence should continue to be directed to the following address:

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By
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